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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,624	10/28/2003	Ulf Tohsche	INFN/0033	6423

7590 11/18/2004

GERO M. McCLELLAN
MOSER, PATTERSON & SHERIDAN, L.L.P.
Suite 1500
3040 Post Oak Blvd.
Houston, TX 77056

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,624	TOHSCHE, ULF	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-20* is/are allowed.

6)☒ Claim(s) *1-4 and 12-14* is/are rejected.

7)☒ Claim(s) *5-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings (filed on 3/25/04) are objected to because Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2. The drawings (filed on 3/25/04) are also objected to because there are minor informalities in the drawings. In particularly, there is an inconsistent between the specification and the drawings because the symbol for logic gate 18 currently shown in Figure 4 and 8 is not for a NAND gate and the specification clearly requires that logic gate 18 is a NAND gate. Note that the symbol of logic gate 18 as currently shown in Figures 4 and 8 is for a NOR gate.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-11 are objected to because of the following informalities:

In claim 1, line 20, "(ii) the logic value" needs to be changed to --(ii) the inverted logic value-- because it is the inverted logic value of the data signal transferred and inverted from the second node to the third node.

Claims 2-11 are objected because they include the informality of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 2, the recitation "a negative-feedback inverter circuit" is indefinite because it is not clear what it means by a negative-feedback inverter circuit.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4, 12-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashita et al. (USP 5,281,865).

With respect to claim 1, Figure 16A discloses a flip-flop which includes: a clock signal (CKB); a data signal (DB); a non-inverted output (QT); and inverted output (QB); a first holding element (1503, 1504) having first (output of 1503) and second (output of 1504) nodes; and a second holding element (1507, 1508) having third (output of 1508) and fourth (output of 1507) nodes; wherein the first node is coupled to the fourth node via a first signal path (MB through 1505) and the second node is coupled to the third node via a second signal path (MT through 1506) exclusive of the first signal path. Note that when CLB = Lo (first level), then the first node having the logic value of the data signal DB while the second node having the logic level of inverted logic value of the data signal DB; and when CLB = Hi (second level), then the logic value DB at the first node transferred and inverted to the fourth node, and the inverted logic value of DB at the second node transferred and inverted to the third node; wherein the fourth node corresponding the non-inverted output and the third node corresponding to the inverted output.

Insofar as understood in claim 2, Figure 16A shows the first and second feedback loops include feed-back inverter circuit.

With respect to claim 3, Figure 16A shows the flip-flop further includes an inverter (1502).

With respect to claim 4, Figure 16A shows the first and second clock-controlled inverters (1505, 1506).

With respect to claim 12, Figure 16A discloses a flip-flop which includes a clock signal (CKB), non-inverted (QT) and inverted (QB) output nodes; data signal (DT); a first holding element (1503, 1504) having first node (output of 1504) and second node (output of 1503); and a second holding element (1507, 1508) having a third node (output of 1507) and a fourth node (output of 1508). Note that when CKB goes to Lo (first edge of the clock), then non-inverted and inverted logic levels of the data signal (DT) are transferred to the first and second node, respectively; and when CKB goes to Hi (second edge of the clock), the non-inverted logic level at the first node is transferred to the non-inverted output node (QT) via the fourth node (i.e., from output of 1504 to the fourth node which is output of 1508 by going through the inverter 1505, and then through the inverter 1507 to QT; note that the propagation delay for this path is two gate delays), and the inverted logic level at the second node is transferred to the inverted output node (QB) via the third node (i.e., from output of 1503 to the third node which is output of 1507, and through the inverter 1508 to QB; node that the propagation delay for this path is two gate delays). Note that the propagation gate delay from the first node to the non-inverted output equals the propagation delay from the second node to the inverted-output as discussed above (both of them having 2 gates delay, i.e., one gate delay for tri-state inverter and one gate delay for regular inverter).

With respect to claims 13 and 14, Figure 16A shows a first signal path between the first node and the non-inverted output node (QT) and a second signal path between the second node and the inverted output node (QB) each comprises the same number of circuit elements (two inverters as discussed in claim 12).

Allowable Subject Matter

8. Claims 5-11are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5 would be allowed because the prior art of record fails to disclose or suggest a flip-flop which includes all the limitations of this claim. In particularly, the prior art of record fails to disclose or suggest that the flip-flop includes, in combination with other limitations, the a reset signal and the second feedback loop comprising a NOR gate having a first input receiving the reset signal.

Claims 6-11 would be allowed because they depend on claim 5.

9. Claims 15-20 are allowed.

Claim 15 would be allowed because the prior art of record fails to disclose or suggest a resettable flip-flop which includes all the limitations of this claim. In particularly, the prior art of record fails to disclose or suggest that the resettable flip-flop includes, in combination with other limitations, the propagation delay of the non-inverted logic level from the first node the non-inverted output node equals to the propagation delay of the inverter level from the second node to the inverted-output node, and the first and second feedback loops each comprises a reset circuitry to place the inverted and non-inverted output nodes at known logic levels in response to a reset signal regardless of the state of the clock signal.

Claims 16-20 would be allowed because they depend on claim 15.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 12, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816